

ABSTRACT

MATRIX ARCHITECTURE FOR DSL APPLICATIONS

A Digital Subscriber Line [DSL] or Very High Speed Digital
Subscriber Line [VDSL] telecommunication device with a downstream
5 path and an upstream path, each path comprising a plurality of
processors interconnected with a plurality of memories. The processors
and the memories are arranged as input/output border column and row
of an interconnecting matrix architecture constituted by
interconnection devices able to interconnect the processors of the
10 column with the memories of the row. This arrangement allows
mapping different architectures simply by changing the status of the
interconnection devices. The matrix arrangement provides a very
flexible simulation platform for different possible applications and,
even when implemented on silicon, the ASIC has a maximum of flexibility
15 and can be adapted to different standard.

Fig. 2 is attached to the abstract.